Power FINFET, a Novel Superjunction Power MOSFET

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Outline

- Overview of Power Semiconductor Devices
- Design issues for Low Voltage Super-Junction Devices
- A Low Voltage Lateral Super-Junction FINFET
  - Basic Idea of SJ-FINFET Structure
  - Device Simulation Works
  - Process Flow and IC Fabrication
  - Experimental Results
- Summary

Applications of Smart Power ICs

Load Current (A)
100
10
1
0.1
0.01
0.001
1
10
100
1000
Supply Voltage (V)

Linear Regulator
Automotive
AC Motors
Switching Regulators
Fluorescent Ballast
Digital
Bipolar linear
Telecom
Display

Worldwide Power Semiconductor Market

$16B

Rev ($M)

LV LV LV LV LV LV

SWR SWR SWR SWR SWR SWR

2006 2007F 2008F 2009F 2010F 2011F

linear Regs, switching regs, references, PM Interface, PM ASIC/ASSP, Rectifiers, Thyristors, LV MOSFETs, HV MOSFETs, IGBTs, Power Bipolar

Source: M. Vukicevic, Data Processing Market to Dominate Power Semiconductor Market in 2007: Market Tracker, iSuppli Corp., Q1, 2007.

HVNMOS process (cont'd)

- Another example of CMOS compatible HV-CMOS with a variety of 40V devices with minimal process changes.

HV *n*-EDMOS: source/body, drain, source

HV *p*-EDMOS: source/body, drain, source

Floating Source HV *n*-FSMOS: source/body, drain, source/body

SiO_2 — p+ n+ — n-drift region — n+ — p-well — Tox = 120Å — p+ — p-drift region — n-well — HV n-well — p-substrate

HV *n*-EDSMOS: source, drain, body

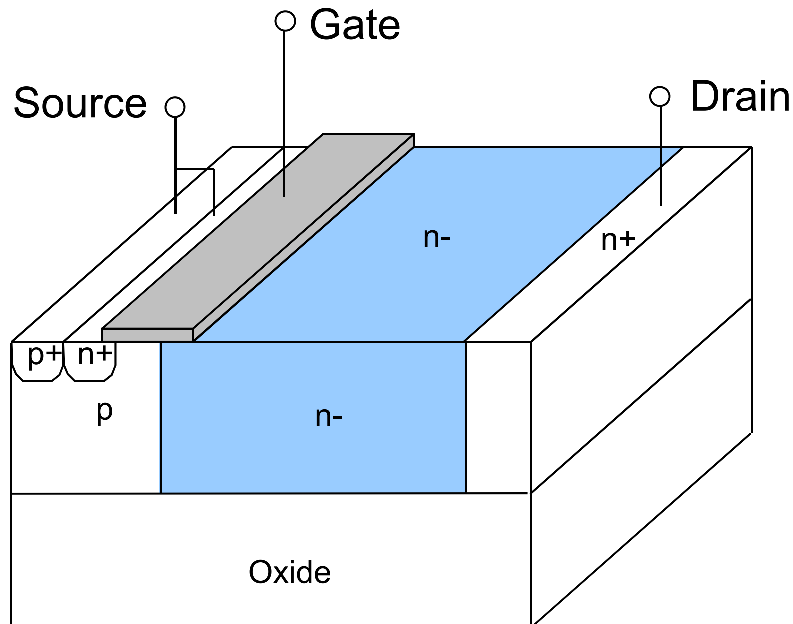
HV *p*-EDSMOS: source, drain, body

Low Voltage CMOS: source/body, drain, source/body

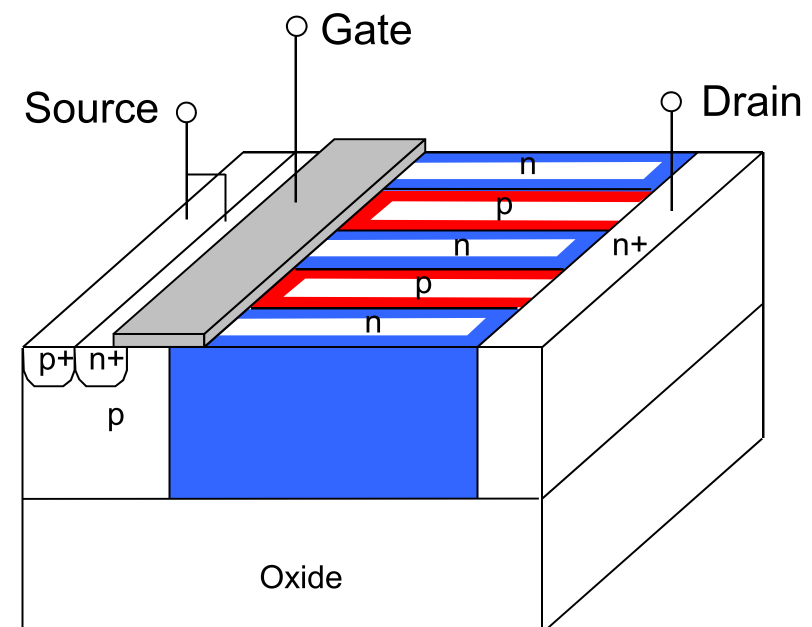
SiO_2 — n+ — n-drift region — p+ — p-well — Tox = 780Å — p-drift region — n-well — p-substrate

Lateral Super-Junction Power MOSFETs

- **Super-Junction** (SJ) power MOSFET is a promising device to achieve a low $R_{on,sp}$ because the drift region is composed of heavily doped alternating n/p-pillars. However, conventional SJ structure is not very attractive for low voltage MOSFETs **(<100V)** due to the fact that the channel resistance becomes comparable to the drift region resistance at low voltage ratings.

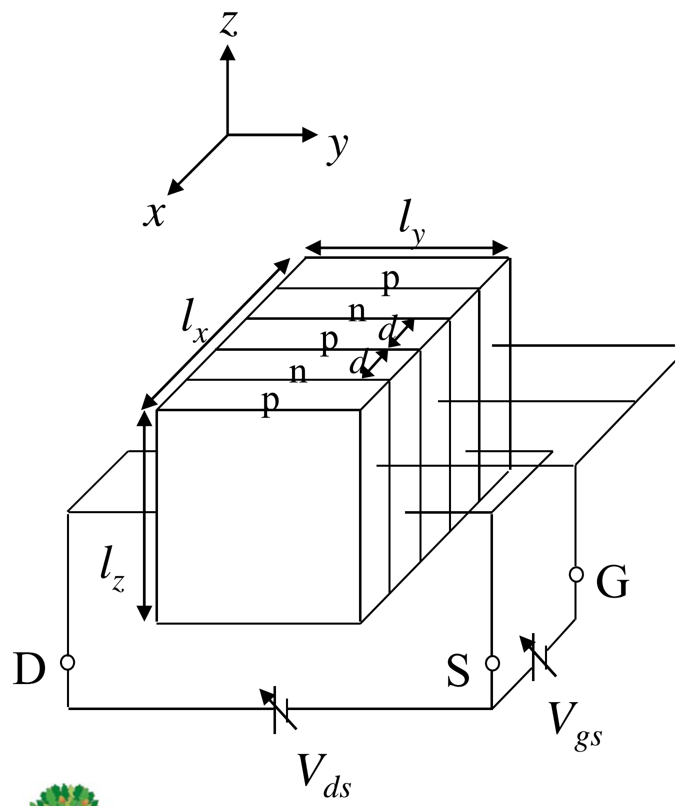


Conventional LDMOSFET



Superjunction LDMOSFET

Impact of the p/n pillar thickness



Si Majority-Carrier Lateral Devices

Specific on-resistance (mΩ cm2)

1000
100
10
1
0.1
0.01
0.001
0.0001

Si-limit

SJ Devices (*Lz* = 10μm)

Si-limit
d=5μm
500nm
50nm

10
100
1000

Breakdown voltage (V)

Fujihira, Fuji, JJAP, 1997

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Features of Super-Junction MOSFETs

- **Drift region structure:** n-drift region replaced by alternatively stacked, charge-coupled/heavily doped, n- and p- thin layers or pillars.
- **Low specific on-resistance:** Current flow only through the heavily doped parallel n-pillars.
- **High breakdown voltage:** requires full-depletion of SJ structures (a space-charged region, acting like a pure intrinsic layer); simply depends on drift region length; independent on dose.
- **Charge counterbalance condition:** controlling the doping of p- and n-type SJ layers according to the RESURF theory.
- **Fabrication process:** complicated and need precise process controls.

Lateral Power Devices – Performance

- BV vs. $R_{on\text{-}sp}$ has been a performance matrix that many researchers have been chasing for years.
- $R_{on\text{-}sp}$ for power devices in the low voltage range (<100V) depends on many factors.

$R_{on,sp}$ [m Ω–cm^2]

10^3
10^2
10^1
10^0
10^{-1}
10^{-2}
10^{-3}

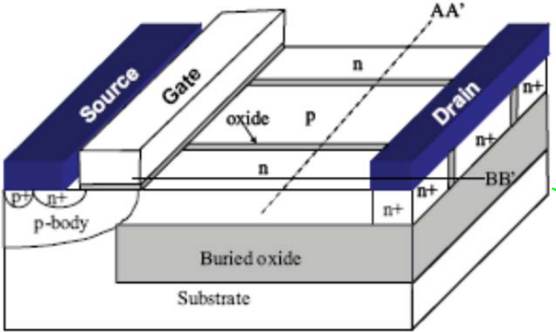
Dual path double-resurf LDMOS[11]
SJ-LDMOS/SOS[13]
Unbalanced SJ-LDMOS[12]
Toshiba-0.8μm CMOS/BESOI[4]
Thick drift LDMOS
BCD5[7]
IDLDMOS[14]
d=5μm
LUDMOS[10]
Motorola[3]

Si_Limit[8],[9]
SJVDMOS[9]
Cool_MOS[9]
SOI
Resurf[2]-[6]
HexLDMOS
Simple Resurf
Data Source

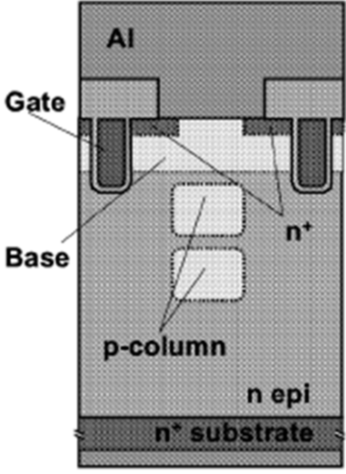
10 100 1000

BV_{dss} [V]

Main Issue: Low Voltage SJ-MOSFETs



Chen et al, NUS, ISPSD, 2007



Miura et al , NEC, ISPSD, 2005

Specific on-resistance ($m\Omega \cdot cm^2$)

100
10
1
0.1
0.01

LDMOS
LDMOS-SOI
LDMOS-SJ
VDMOS
VDMOS-SJ
Si-limit

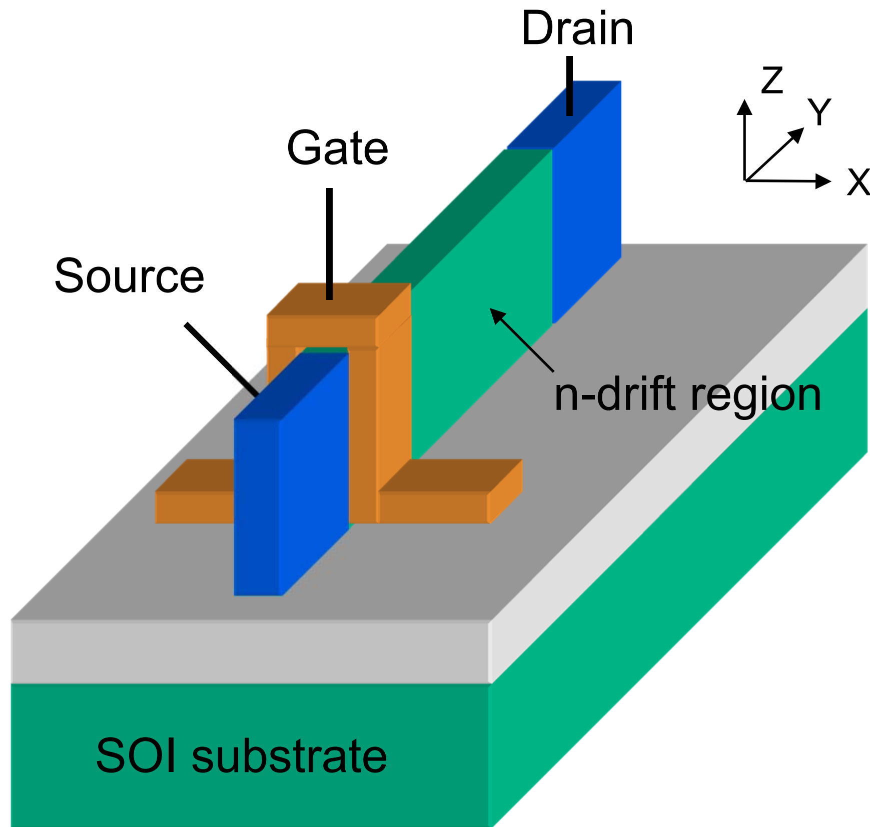
Sub-200V

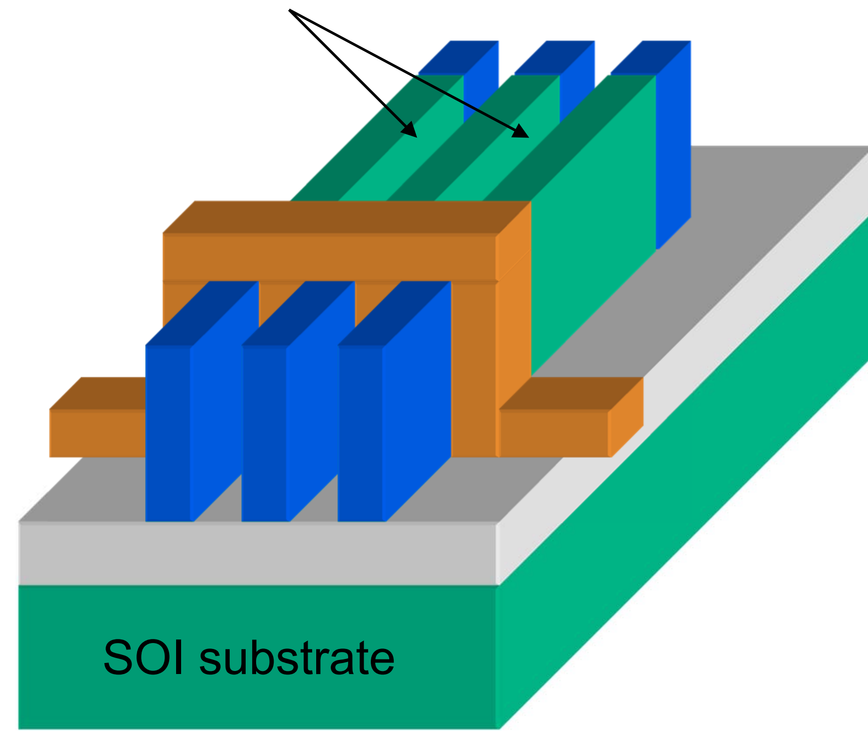
Si-limit

10
100
1000

Breakdown voltage (V)

Basic Idea of SJ-FINFET Structure



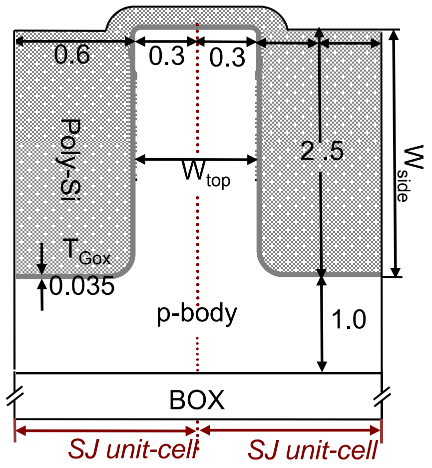


- Reduction of channel resistance
- Reduction of n-drift resistance
- E-field relaxation (i.e. higher BV)
- More efficient use of silicon

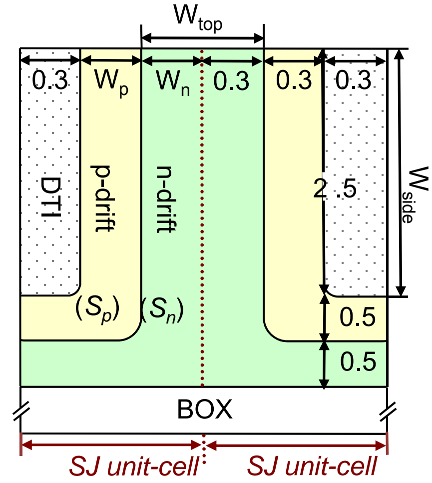
Proposed Lateral SJ-FINFET Structure

Z Y X
Gate A' B' Drain
W_{top}
C C'
n W_n
p n+
Source n+ DTI
p W_p
n $2{\cdot}W_n$
L_{ch} L_{drift}
n+ W_{side} n+
p-body T_{epi}
A B
p+
BOX
p-substrate
SJ unit-cell

Cross-section: A-A'

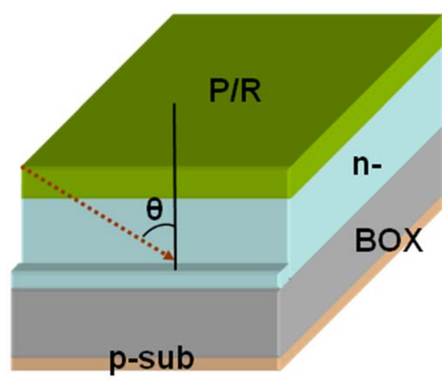


Cross-section: B-B'

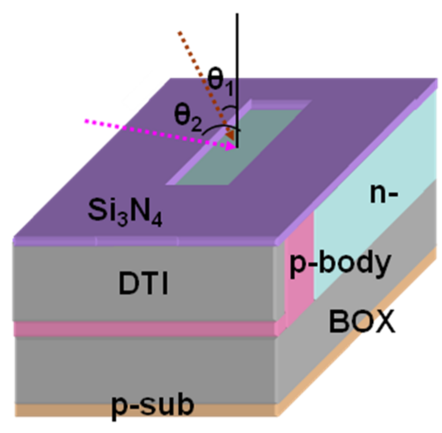


- Compatibility with modern CMOS process is an essential design consideration

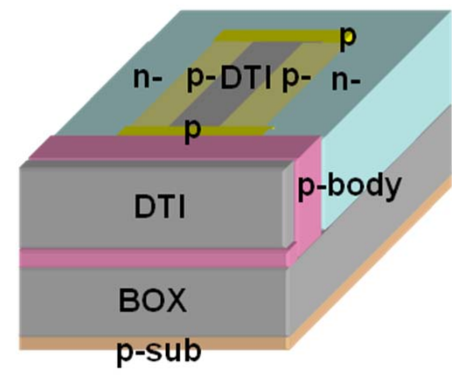
Process Flow for the SJ-FINFET Structure



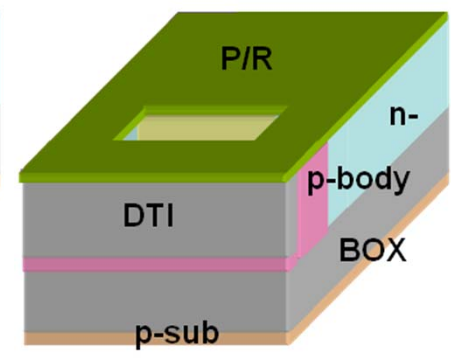
(a) p-body implant



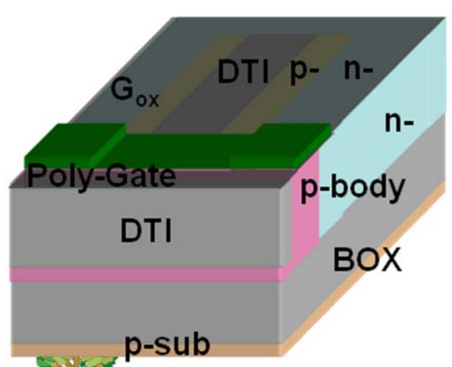
(b) SJ-drift trench & implant



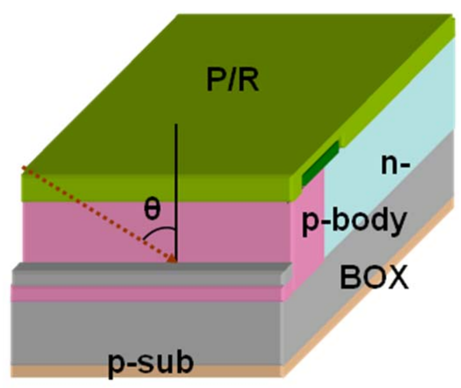
(c) p-pillar diffusion



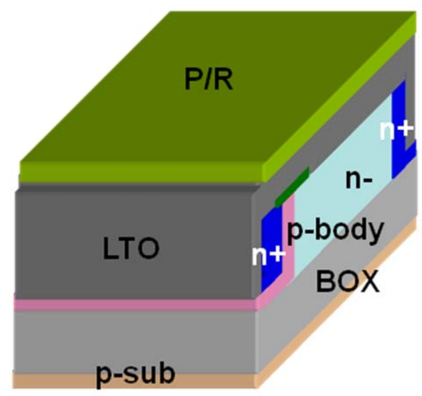
(d) gate trench



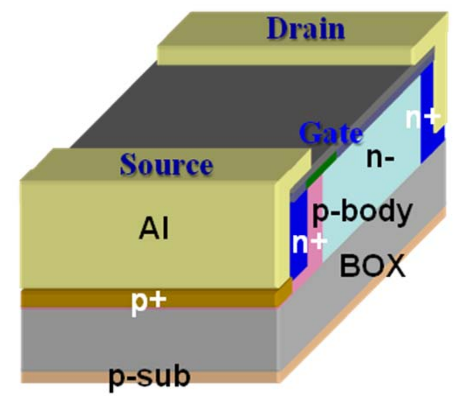
(e) n-doped poly-Si gate



(f) n+ source implant



(g) p+ contact opening



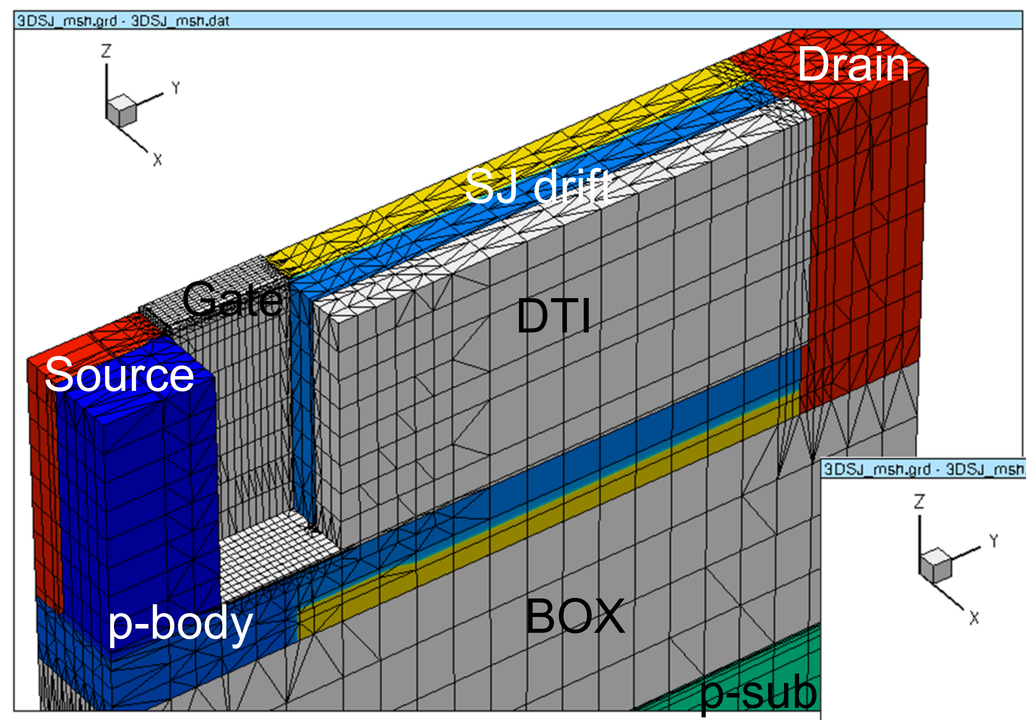
(h) Al metallization

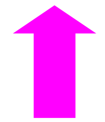
Parameters for 3D Simulations

- These parameters were also used in the fabrication of the prototypes.

Parameters	Values
Drift length, L_{drift} (μm)	3 to 12
n-drift width, W_n (μm)	0.6
n-drift doping conc., N_D (cm^{-3})	7.4×10^{16}
p-drift width, W_p (μm)	0.3
p-drift doping conc., N_A (cm^{-3})	7.4 to 9.8×10^{16}
p-body doping conc., $N_{p\text{-}body}$ (cm^{-3})	5.0×10^{17}
p-substrate doping conc., N_{sub} (cm^{-3})	2.0×10^{14}
n+ source/drain contact, $N_{s/d}$ (cm^{-3})	1.0×10^{20}
p+ contact, N_{p+}(cm^{-3})	5.0×10^{19}
Gate oxide thickness, T_{Gox} (nm)	35
Top channel width, W_{top} (μm)	0.6
Side channel width, W_{side} (μm)	2.0 and 3.0
Gate length, L_{gate} (μm)	1.0
Channel length, L_{ch} (μm)	0.5
SOI thickness, T_{epi} (μm)	2.6 and 3.6
DTI depth (μm)	2.0 and 3.0
Buried oxide thickness, T_{box} (μm)	2.0

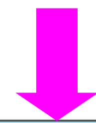
SJ-FINFET — Initial MESH Structure

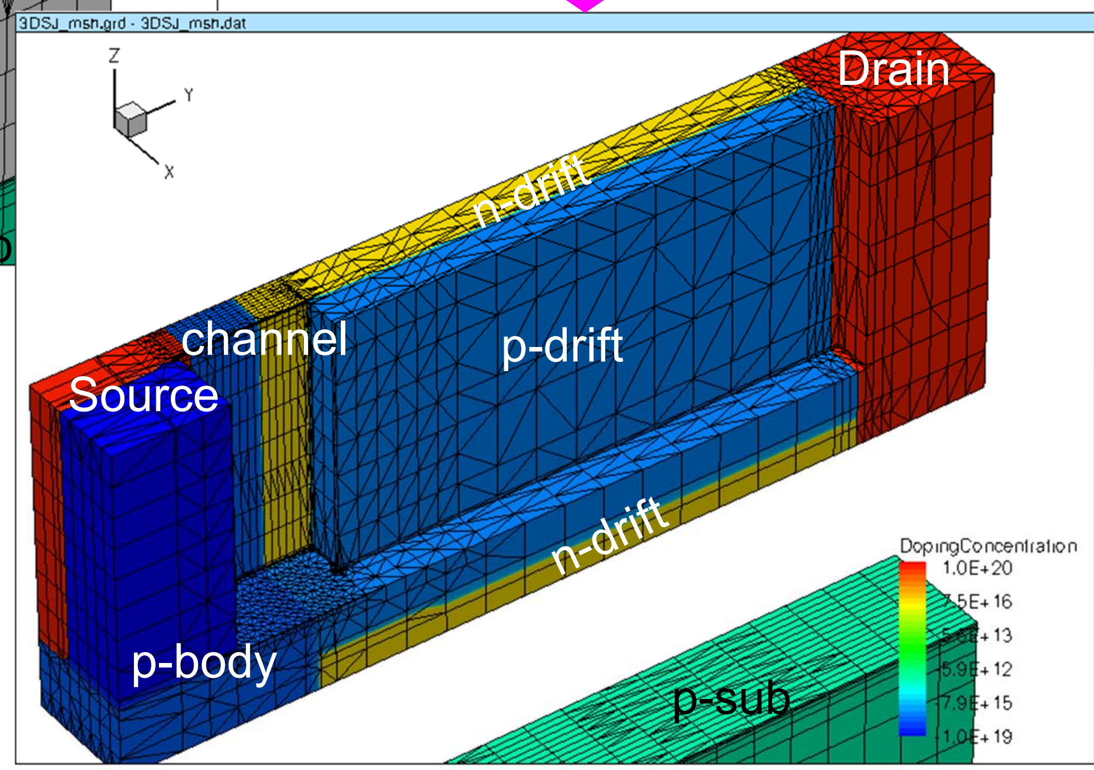




- SJ unit-cell (w/ DTI & Gox)

- SJ unit-cell (w/o DTI & Gox)





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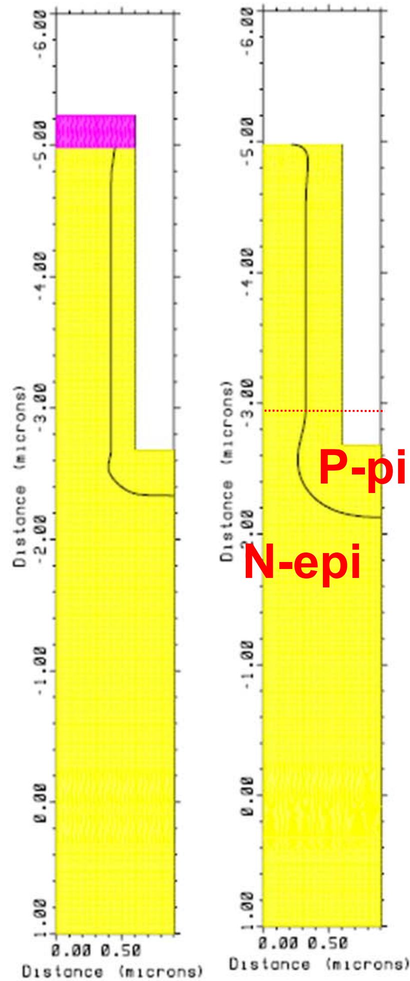
Formation of the p/n pillars

Implant **After annealing**



@ Y = -3

B, 8e13 cm^{-2}, 45 keV, ± 12°

Log10(active(arsenic))

Boron

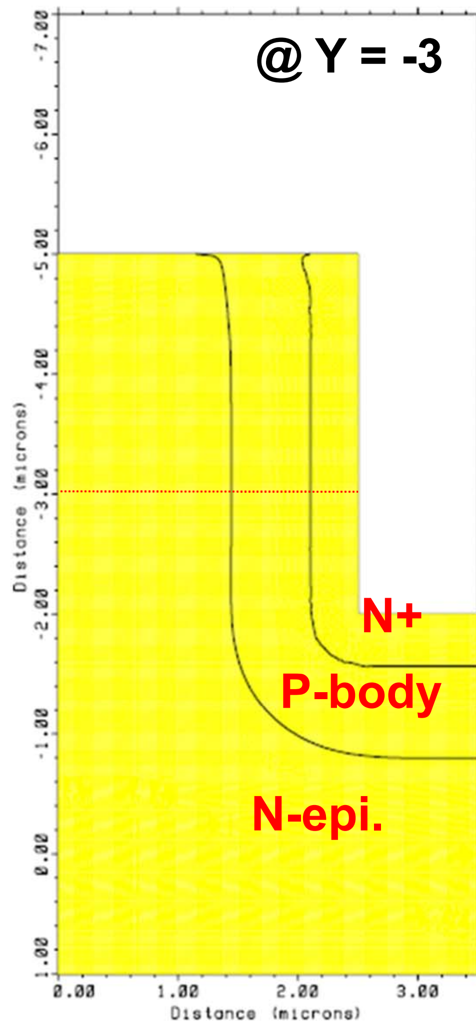
N-epi

P-pillar

Phosphorus

Distance (microns)

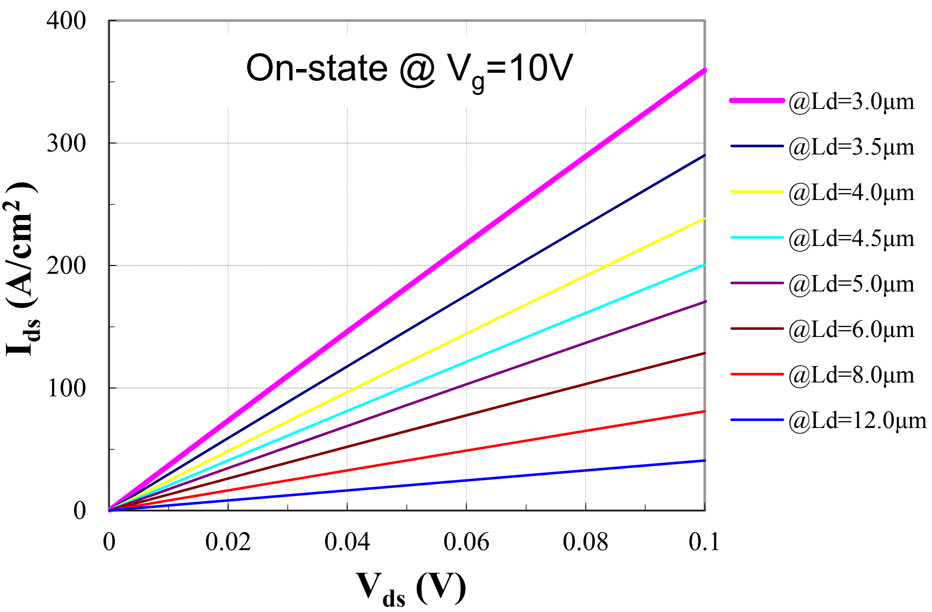
Formation of the n+ source/drain contacts

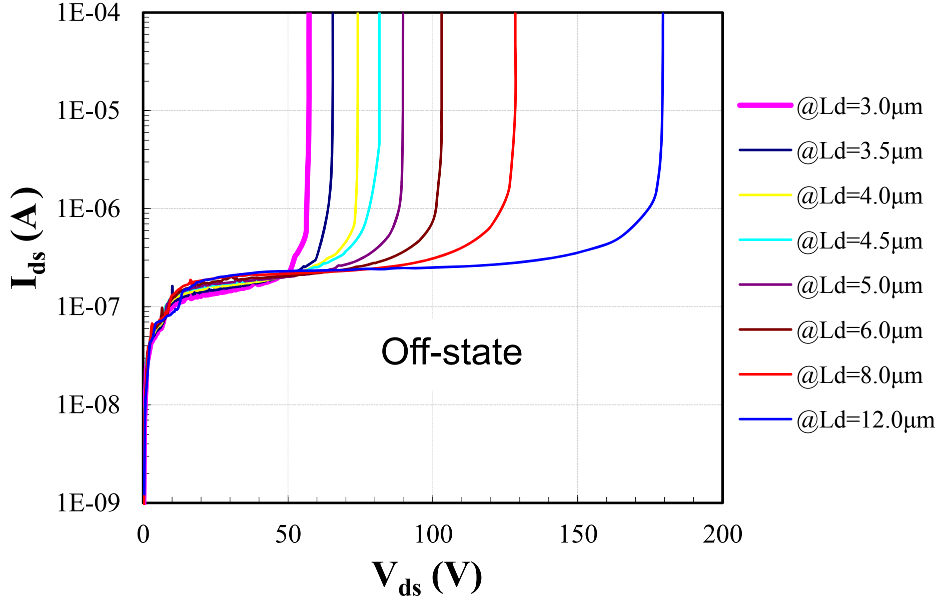


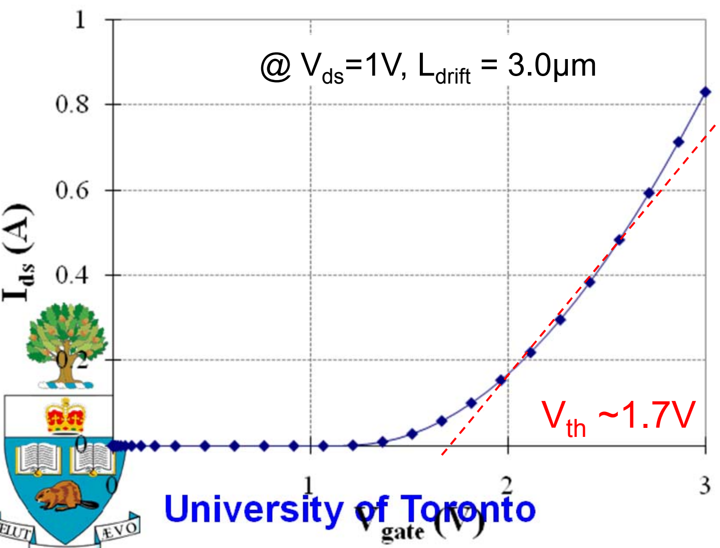
P, 5e14 cm^{-2}, 180 keV, ± 45°
As, 9e14 cm^{-2}, 200 keV, ± 45°

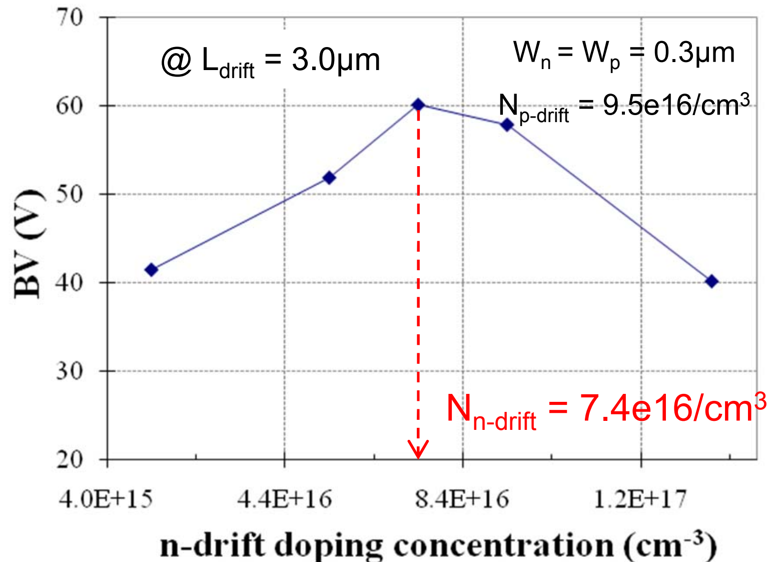
N+
Phosphorus
P-body
N-epi
Arsenic
Boron
log10(active(arsenic))
Distance (microns)

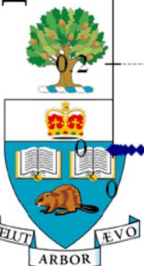
SJ-FINFT — Device Simulation Results











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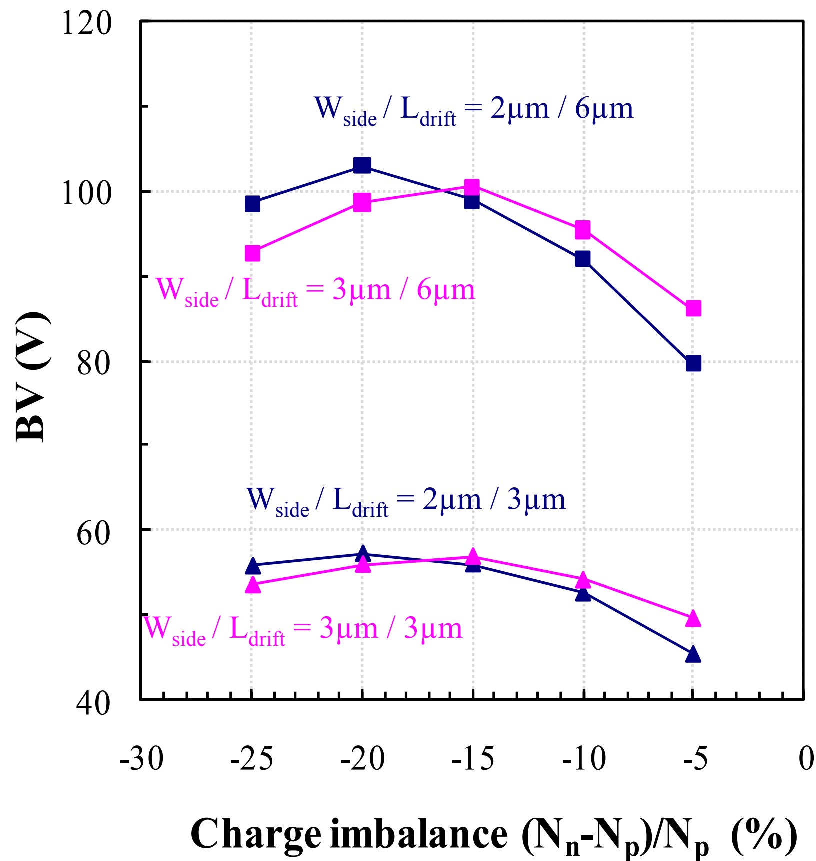
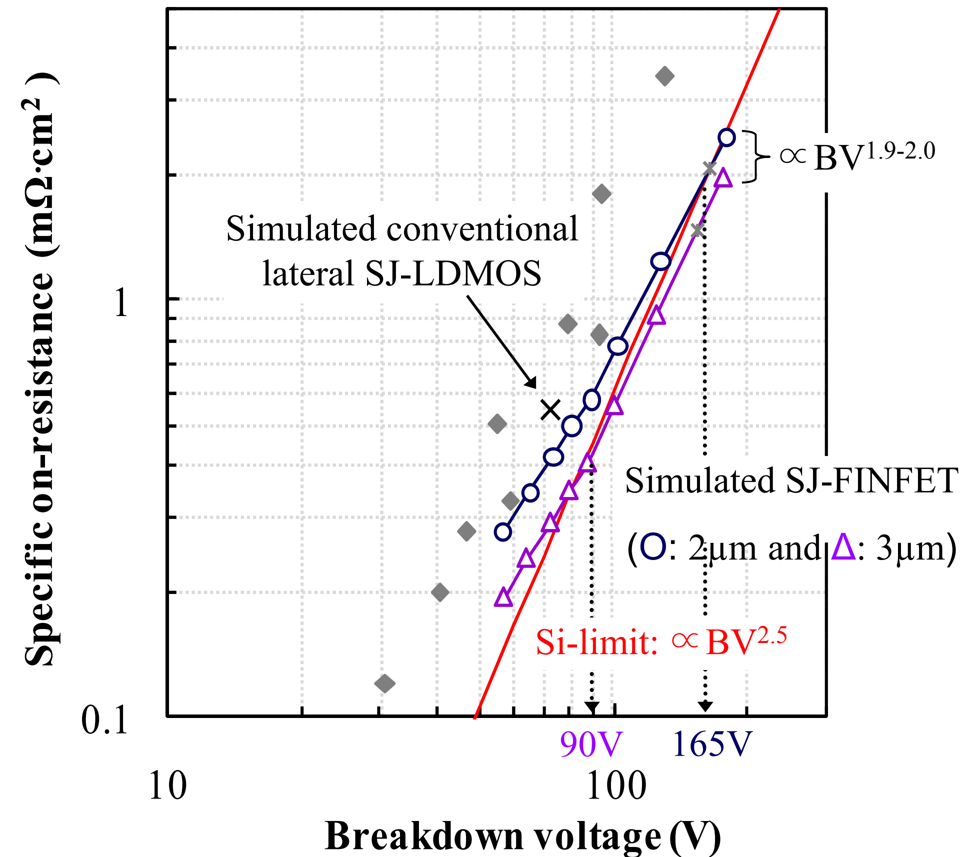
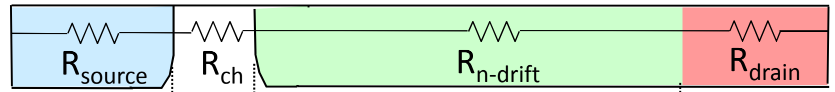
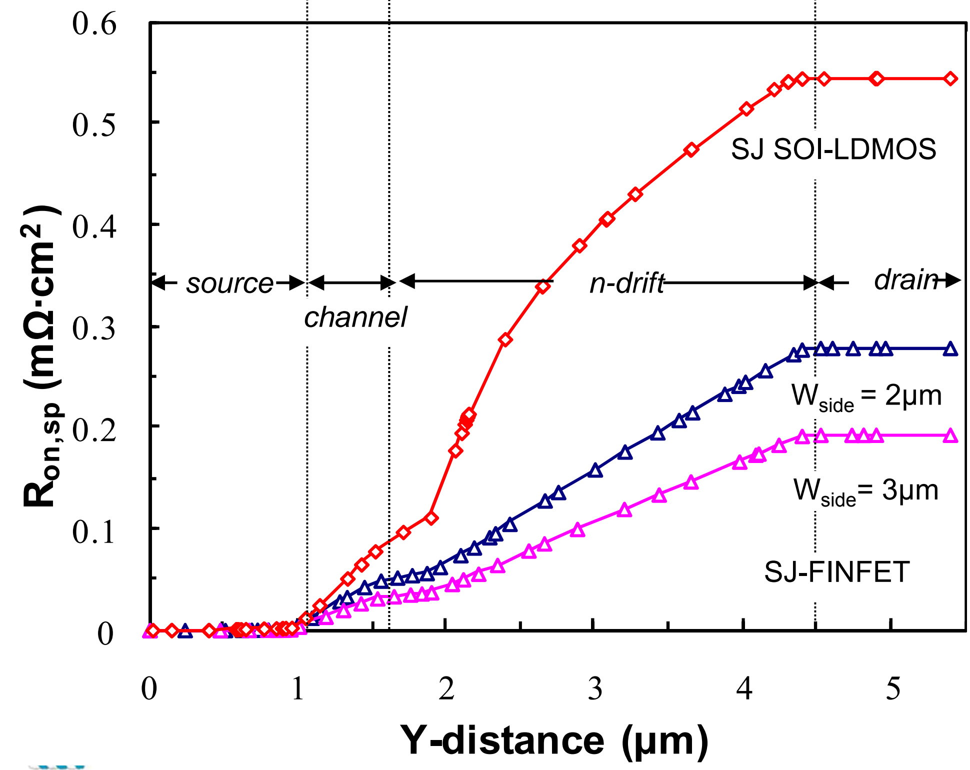
SJ-FINFT — Device Simulation Results (cont'd)



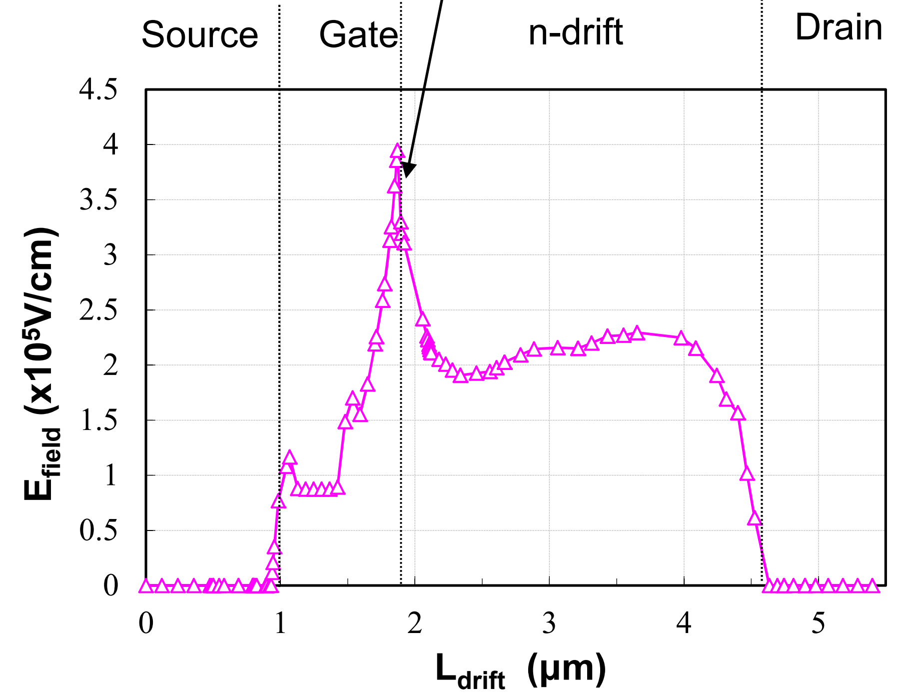


SJ-FINFT — Device Simulation Results (cont'd)





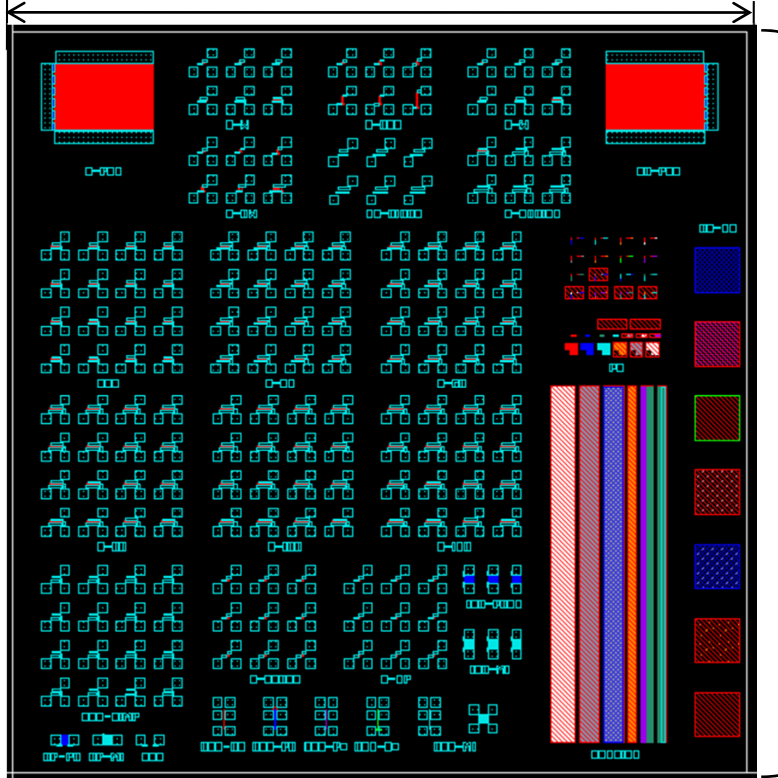
- Relaxing the electric field at this point achieves higher breakdown voltage



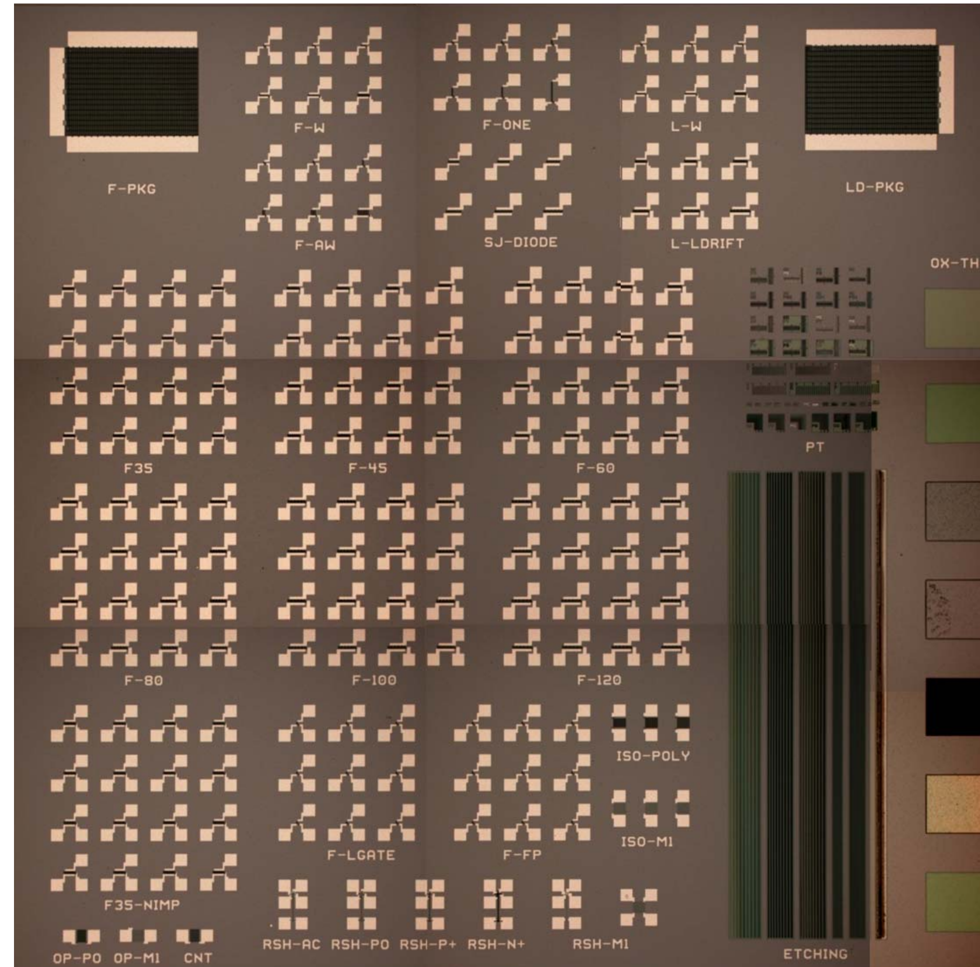
E_c for Si ~ 5 x 10^5 V/cm, BV~($E_c \cdot L_{drift}$) / 2

Final Chip Layout & Die Image

50000µm (Mask=5cm, Die=1cm)

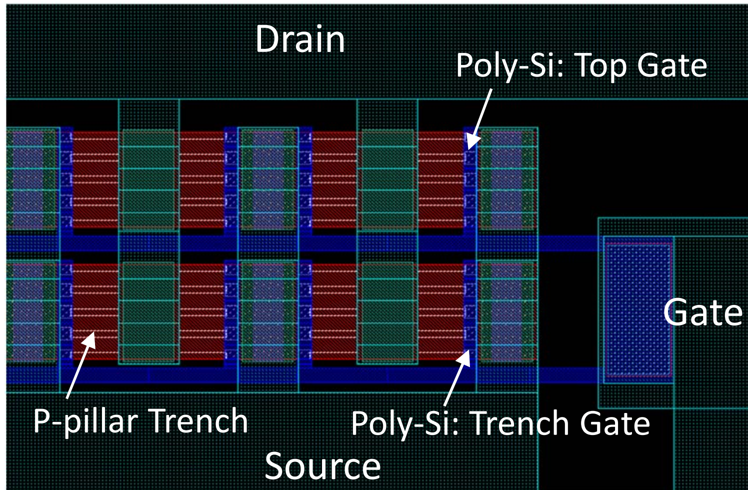


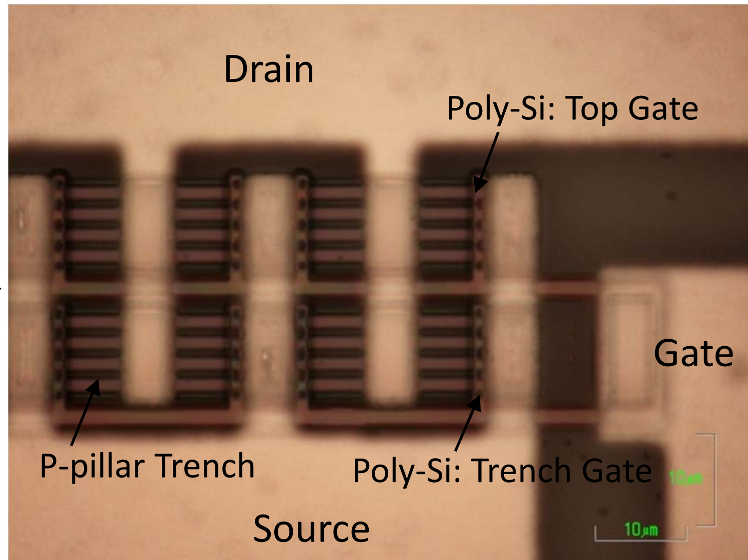
50000µm (Mask=5cm, Die=1cm)

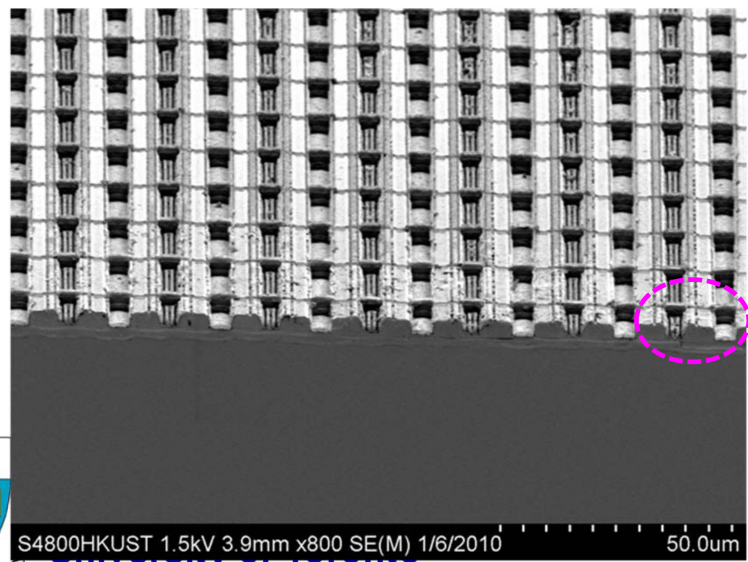


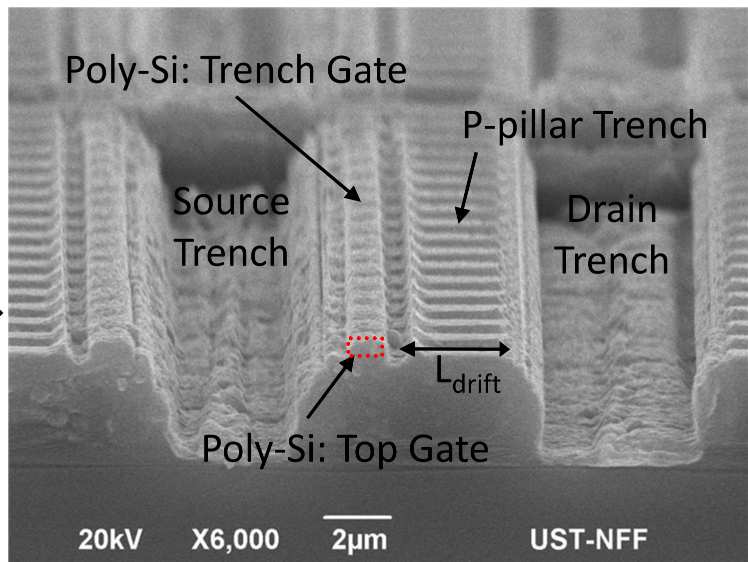
- Total 9 Mask Layers

Fabricated SJ-FINFETs: Optical & SEM Images

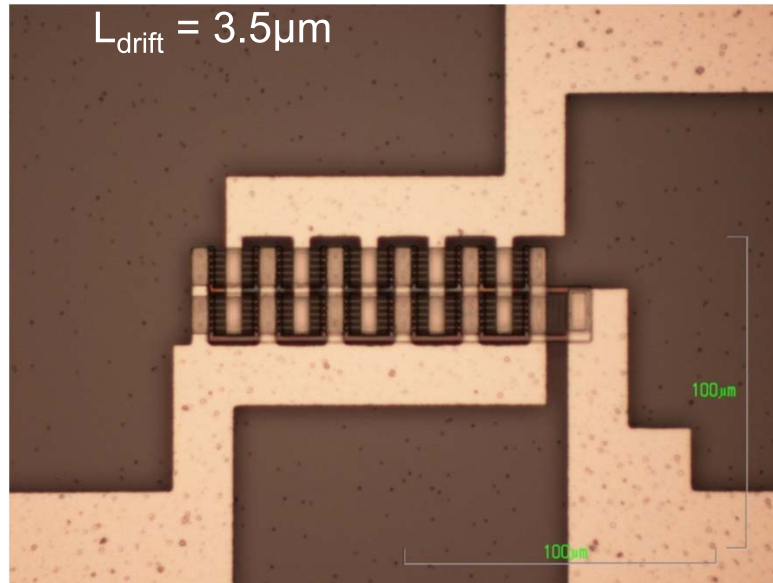


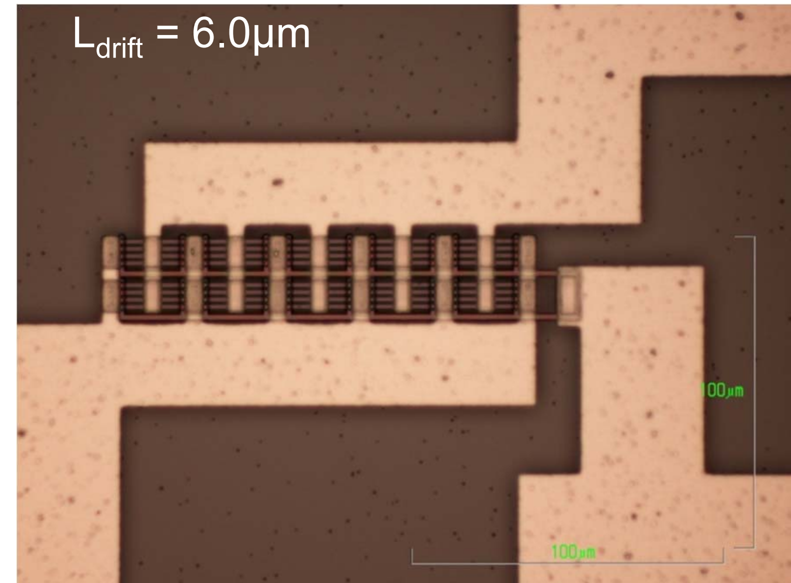


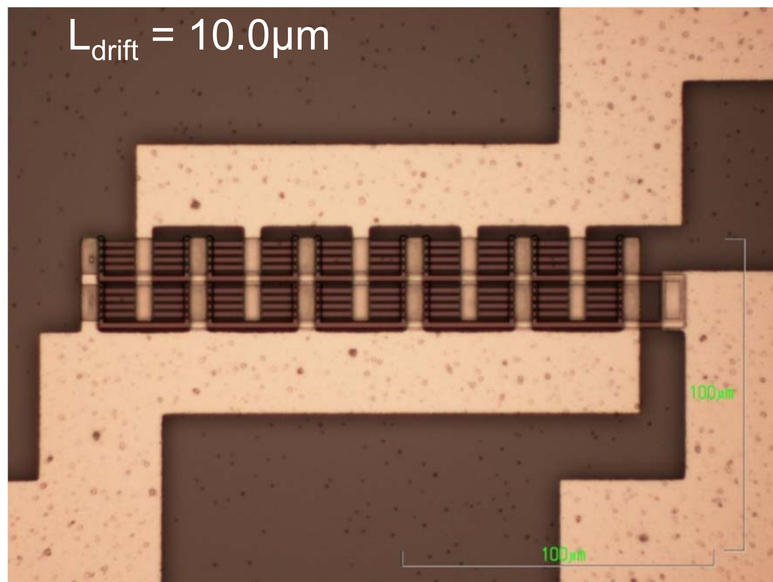


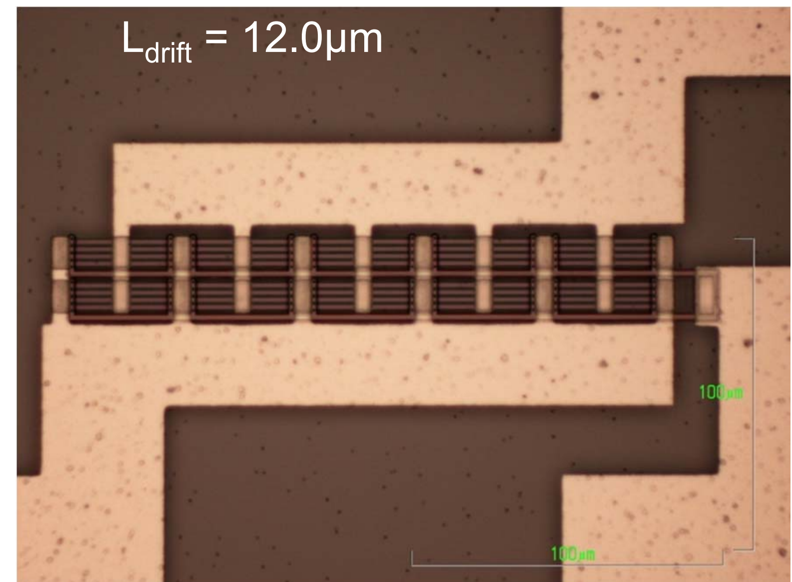


SJ-FINFETs: After Al-Metallization









Measured Data: Transfer I-V Characteristics

- L_{drift}=3.5µm, W=200µm, T_{ox} = 35nm @ V_{ds} = 0.1V

I_{ds} (A)

6E-03
5E-03
4E-03
3E-03
2E-03
1E-03
0E+00

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

V_{gate} (V)

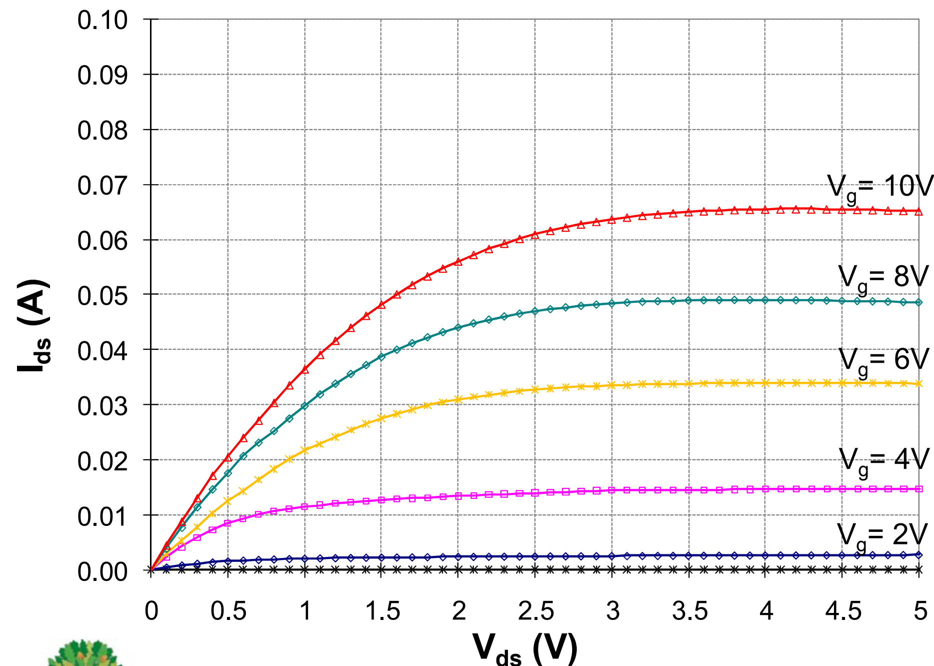
V_{th} ~ 1.7V

- The measured threshold voltage of the SJ-FINFET was approximately 1.7V

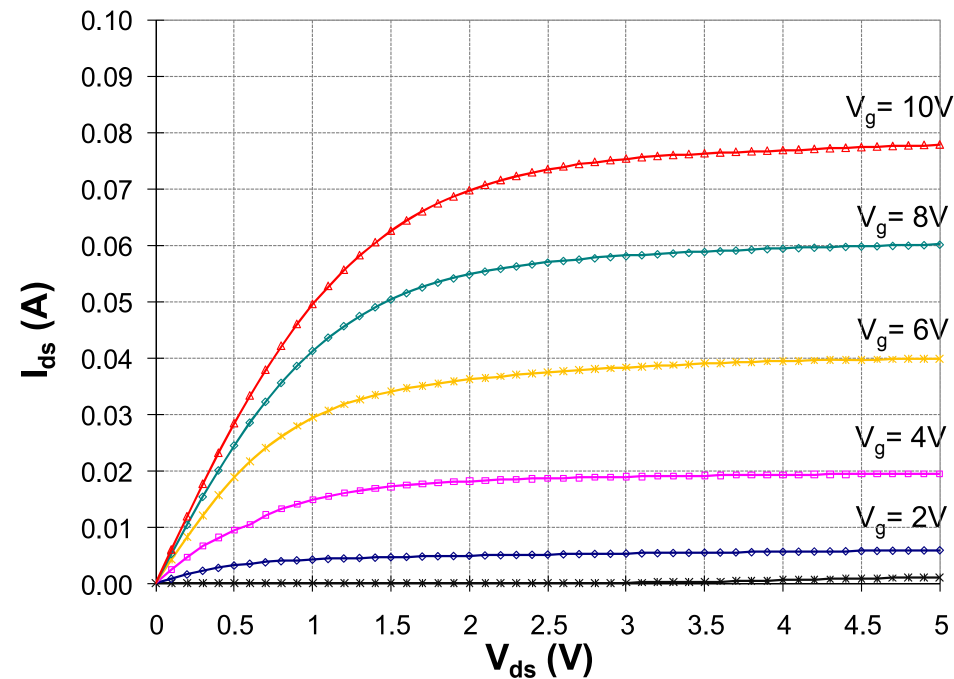
Measured Data: Output I-V Characteristics

- The $R_{on,sp}$ of the SJ-FINFET is approximately 30% smaller than that of the conventional SJ-LDMOSFET.

- SJ-LDMOS: L_{drift}=3.5μm, W=200μm

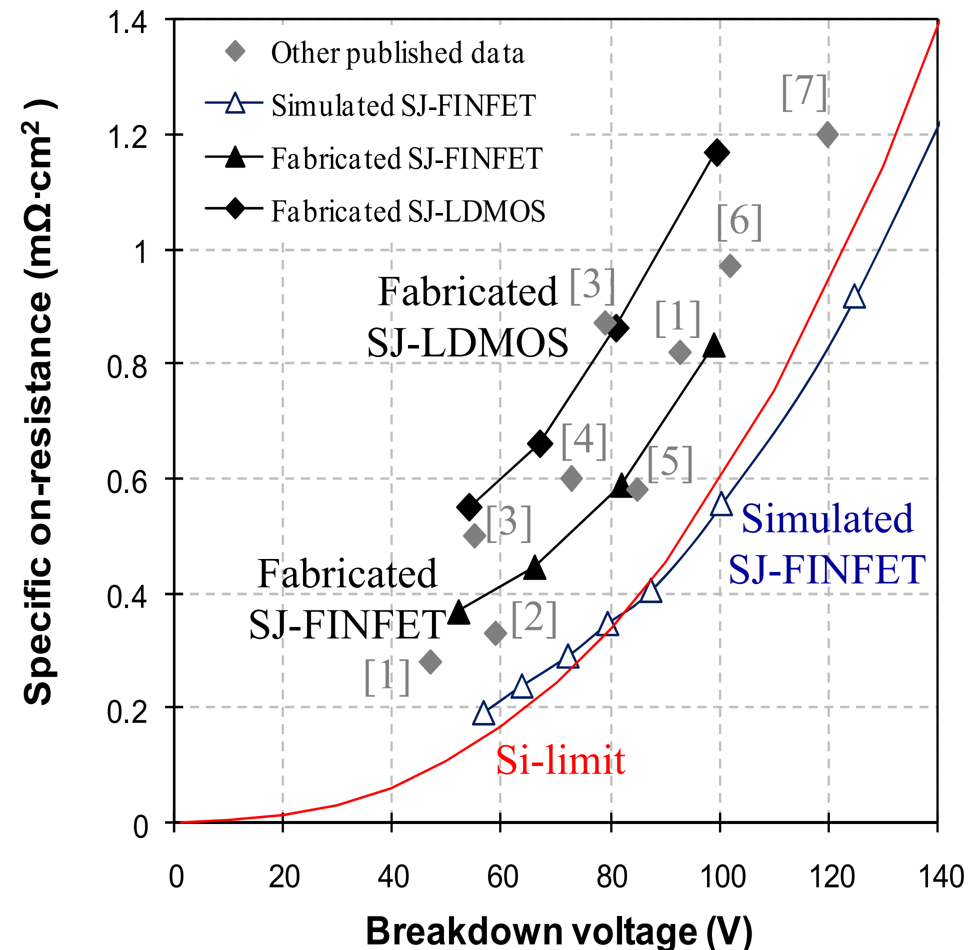


- SJ-FINFET: Ldrift=3.5μm, W=200μm



Measured Data: BV versus $R_{on,sp}$

- The measured data is comparable with other published data and it shows a good agreement in the data trend between the simulation and measurement. For similar BV ratings, about 30% lower $R_{on,sp}$ was found in the fabricated



Data from [1], [3], [7] are for conventional LDMOSFETs

Data from [2], [4]-[6] are for conventional SJ-LDMOSFETs

Summary

- Low voltage lateral SJ-FINFET devices with deep trench p-drift region were proposed and fabricated to improve the electrical characteristics of conventional planar gate SJ-LDMOSFETs.
- For the similar BV ratings, the specific on-resistances of the fabricated SJ-FINFET devices were approximately 30% lower than that of the fabricated SJ-LDMOSFETs.
- The current work represents the first experimental confirmation that the super-junction concept is advantageous for sub-200V applications.
- More details will be presented at IEDM 2010.

Acknowledgements

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- Natural Sciences and Engineering Research Council of Canada
- U of T Open Fellowship